APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Daisuke Kawagoe	Examiner: Ishwar B. Patel
Serial No.: 10/646,478	Group Art Unit: 2841
Filed: August 22, 2003	Docket: 884.937US1

For: STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

APPEAL BRIEF UNDER 37 CFR § 41.37

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in response to the Notice of Panel Decision from Pre-Appeal Brief Review mailed on March 5, 2007 and further in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on May 31, 2006, from the Final Rejection of claims 40-58 of the above-identified application, as set forth in the Final Office Action mailed on March 21, 2006.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.20(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present application was filed on August 22, 2003 with claims 1-21. A non-final Office Action was mailed January 12, 2005, and claims 1-21 were canceled and claims 22-39 were added in the response to the Office Action. A Final Office Action was mailed on June 29, 2005, claims 22-39 were canceled and claims 40-58 were added in the response to Office Action with a Request for Continued Examination (RCE). A second non-final Office Action was mailed November 15, 2005. A second Final Office Action (hereinafter "the Final Office Action") was mailed March 21, 2006. Claims 40-58 stand twice rejected, remain pending, and are the subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated March 21, 2006.

5. SUMMARY OF CLAIMED SUBJECT MATTER

FIG. 1 and the specification at page 2, lines 13-24 illustrate and describe a substrate 10 in accordance with one example embodiment of the invention. The substrate 10 includes a first dielectric layer 22A, a second dielectric layer 22B and a third dielectric layer 22C such that the second dielectric layer 22B is between the first and third dielectric layers 22A, 22C. The first, second and third dielectric layers 22A, 22B, 22C are formed on a core 20.

A first conductive layer 24B is between the first and second dielectric layers 22A, 22B and a second conductive layer 24C is between the second dielectric layer 22B and the third dielectric layer 22C. The second conductive layer 24C includes a first skip via 21A that extends through the first and second dielectric layers 22A, 22B.

A third conductive layer 22C is on the third dielectric layer 22C. The third conductive layer includes a second via 21B that extends through the third dielectric layer 22C such that the second via 21B and the first skip via 21A are stacked on top of one another.

As used herein, vias that are stacked refers to vias that at least partially overlap. In some embodiments, the longitudinal axis of each via may be substantially aligned with the longitudinal axis of the other vias.

FIGS. 2 and 3 and the specification at page 2, line 25 through page 3, line 12 illustrate and describe a substrate 10 in accordance with another example embodiment of the invention. The substrate 10 includes a first dielectric layer 22A, a second dielectric layer 22B and a third dielectric layer 22C such that the second dielectric layer 22B is between the first and third dielectric layers 22A, 22C. The substrate 10 further includes a fourth dielectric layer 22D such that the third dielectric layer 22C is between the second and fourth dielectric layers 22B, 22D. The first, second, third and fourth dielectric layers 22A-D are formed on a core 20.

A first conductive layer 24B is between the first and second dielectric layers 22A, 22B and a second conductive layer 24C is between the second dielectric layer 22B and the third dielectric layer 22C. The second conductive layer 24C includes a first skip via 21A that extends through the first and second dielectric layers 22A, 22B.

A third conductive layer is between the third and fourth dielectric layers 22C, 22D and a fourth conductive layer is on the fourth dielectric layer 22D. The fourth conductive layer

includes a second skip via 21B that extends through the third and fourth dielectric layers 22C, 22D such that the second skip via 21B and the first skip via 21A are stacked on top of one another.

Utilizing one or more skip vias in a stack of vias reduces the number of via-to-via interfaces within the stack of vias. The via-to-via interfaces within a stack of vias are the sections within the stack of vias that tend to crack or delaminate when the vias are subjected to stress. Therefore, reducing the number of via-to-via interfaces within the stack of vias may make electronic assemblies that include such substrates less likely to fail.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 40-44 were rejected under 35 USC § 102(e) as being anticipated by Carpenter (U.S. 6,810,583).

Claims 47-51 were also rejected under 35 USC § 102(e) as being anticipated by Carpenter.

Claims 54-56 were rejected under 35 USC § 103(a) as being unpatentable over Carpenter.

Claims 45, 46, 52, 53, 57 and 58 were also rejected under 35 USC § 103(a) as being unpatentable over Carpenter, and further in view of Uchikawa (U.S. 6,531,661) and Asai (U.S. 6,534,723).

7. ARGUMENT

A) The Applicable Law under 35 U.S.C. §102

A claim is anticipated only if each and every element set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *M.P.E.P. ' 2131.* To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. V. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

B) Discussion of the rejection of claims 40-44 under 35 USC § 102(e) as being anticipated by Carpenter (U.S. 6,810,583).

As part of making the rejection, the Examiner states at page 2 of the Final Office Action that

> "Carpenter, in figure 6, discloses a substrate comprising: . . . a second conductive layer (C2 , as marked up on figure 6 in appendix "A"); between the second dielectric layer and the third dielectric, the second conductive layer including a first skip via (57) that extends through the first and second dielectric layers; and a third conductive layer (C3) on the third dielectric layer, the third conductive layer including a second via (26) that extends through the third dielectric layer, the second via and the first skip via being stacked on to of one another (see marked up figure 6 in appendix "A")."

Applicant respectfully traverses these assertions. The Examiner's marked up drawing shows that the layer C2 (indicated by the Examiner as the second conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C2 layer. Applicant further notes that each of vias 55, 56, 57, 58 in Carpenter are shown with separate cross-hatching from the corresponding metallizations 21, 31, 28, 29 in the metallic layer 14. Since the vias 55, 56, 57, 58 in Carpenter are not part of the metallic layer 14 (indicated as the C2 layer by the Examiner), Carpenter does not teach or suggest "the second

conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 40.

Applicant also respectfully submits that the Examiner's marked up drawing shows that the layer C3 (indicated by the Examiner as the third conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C3 layer. Therefore, Carpenter does not teach or suggest "the third conductive layer including a second via that extends through the third dielectric layer" as recited in claim 40.

The Examiner further states at page 13 of the Final Office Action that

> "The applicant argues that layer C2 (second conductive layer) does not include any vias. Therefore, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers". This is not found to be correct. Via (57) as shown in marked up figure 6 (appendix "A"), does extend through dielectric layer Dl and D2 and is connected with the conductive layer (C2)."

Applicant respectfully traverses these assertions in part because even though via 57 extends through dielectric layers D1 and D2 (reference numbers 41 and 43 in Carpenter), and is connected to metallization 28 in metallic layer 14, the via 57 is not part of the metallic layer 14 as indicated by the separate cross-hatching in Figure 6. Applicant notes that the dielectric layer 41 is connected to the metallic layer 14, but Applicant respectfully submits that just as with via 57, the dielectric layer 41 is NOT part of metallic layer 14. Since the vias 55, 56, 57, 58 in Carpenter are not part of the metallic layer 14, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 40.

The Examiner also states at page 13 of the Final Office Action that

> "Applicant further argues that layer C3 (third conductive layer in marked up figure 6 (appendix "A") does not include any via. Therefore, carpenter does not teach or suggest "the third conductive layer including a second via that extends through the third dielectric layer". This is not found to correct. Via (26) as shown in marked up figure 6 (appendix "A"), does extend through the dielectric layer D3 and is connected with the conductive layer (C3)."

Applicant respectfully traverses these assertions in part because even though via 26 extends through dielectric layer D3 (reference numbers 13 and 15 in Carpenter), and is

connected to metallization 87 in metallic layer 116, the via 26 is not part of the metallic layer 116 as indicated by the separate cross-hatching in Figure 6. Applicant notes that the dielectric layer 15 is connected to the metallic layer 116, but Applicant respectfully submits that just as with via 26, the dielectric layer 15 is NOT part of metallic layer 116. Since none of the vias in Carpenter are part of any metallic layer, Carpenter does not teach or suggest "the third conductive layer including a second via that extends through the third dielectric layer" as recited in claim 40.

C) Discussion of the rejection of claims 47-51 under 35 USC § 102(e) as being anticipated by Carpenter.

As part of making the rejection, the Examiner states at page 4 of the Final Office Action that

> "Carpenter, in figure 7, discloses a substrate comprising: . . . a second conductive layer (C3, marked up on figure 7 in appendix "B") between the second and third dielectric layers, the second conductive layer including a first skip via (VI, marked up on figure 7 in appendix "B") that extends through the first and second dielectric layers; a fourth dielectric layer (D4, marked up on figure 7 in appendix "B"), the third dielectric layer being between the second and fourth dielectric layers; a third conductive layer (C4, marked up on figure 7 in appendix "B") between the third and fourth dielectric layers; and a fourth conductive layer (C5, marked up on figure 7 in appendix "B") on the fourth dielectric layer, the fourth conductive layer including a second skip via (V2, marked up on figure 7 in appendix "B") that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another (see marked figure 7 in appendix "B")."

Applicant respectfully traverses these assertions. The Examiner's marked up figure 7 shows that the layer C3 (indicated by the Examiner as the second conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the metallizations in the marked C3 layer. Applicant further notes that each of vias in Carpenter is shown with separate cross-hatching from the corresponding metallizations in the metallic layer C3. Since the vias in Carpenter are not part of the metallic layer (indicated as the C3 layer by the Examiner), Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 47.

Applicant also respectfully submits that the Examiner's marked up figure 7 shows that the layer C5 (indicated by the Examiner as the fourth conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C5 layer. Applicant further notes that each of vias in Carpenter is shown with separate cross-hatching from the corresponding metallizations in the metallic layer C5. Therefore, Carpenter does not teach or suggest "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers" as recited in claim 47.

The Examiner further states at page 13 of the Final Office Action that

> "Similarly regarding the independent claim 47, the applicant argues that Carpenter does not disclose or teach the second conductive layer including a first skip via that extends through the first and second dielectric layers and the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers. This is not found to be correct. Via (V1, as shown in figure 7, appendix B) extend through dielectric layers D1 and D2 and is connected to conductive layer C3. Similarly Via (V2) extend through dielectric layer D3 and D4 and connected to conductive layer C5."

Applicant respectfully traverses these assertions in part because even though via V1 (as indicated by the Examiner in marked up Figure 7) extends through dielectric layers D1 and D2, and is connected to a metallization in metallic layer C3, the via V1 is NOT part of the metallic layer C3 as indicated by the separate cross-hatching in Figure 7. Applicant notes that the dielectric layer D2 is connected to the metallic layer C3, but Applicant respectfully submits that just as with via V1, the dielectric layer D2 is NOT part of metallic layer C3. Since the via V1 in Carpenter is not part of the metallic layer C3, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 47.

Applicant also respectfully traverses these assertions in part because even though via V2 (as indicated by the Examiner in marked up Figure 7) extends through dielectric layers D3 and D4, and is connected to a metallization in metallic layer C5, the via V2 is NOT part of the metallic layer C5 as indicated by the separate cross-hatching in Figure 7. Applicant notes that the dielectric layer D4 is connected to the metallic layer C5, but Applicant respectfully submits that just as with via V2, the dielectric layer D4 is NOT part of metallic layer C5. Since the via

V2 in Carpenter is not part of the metallic layer C5, Carpenter does not teach or suggest "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another" as recited in claim 47.

D) The Applicable Law under 35 U.S.C. §103(a)

To sustain a rejection under 35 U.S.C. 103, references must be cited that teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02.

Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). The Office Action must further provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).

E) Discussion of the rejection of claims 54-56 under 35 USC § 103(a) as being unpatentable over Carpenter.

As part of making the rejection, the Examiner states at page 6 of the Final Office Action that "Carpenter discloses all the features of the claimed invention as applied to claim 47 above,"

Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" or "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers" as recited in claim 47.

Claims 54-56 depend from claim 47 such that claims 54-56 incorporate all of the limitations of claim 47. Therefore, claims 54-56 are allowable for the reasons provided above with regard to claim 47.

The Examiner further states at page 6 of the Final Office Action that

> "It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the third skip via connected to the sixth conductive layer, in order to have desired electric connection for signal, power or ground."

Applicant respectfully traverses this assertion and notes that the cited reference has no teaching or suggestion as to any of the conductive layers including a via.

F) Discussion of the rejection of claims 45, 46, 52, 53, 57 and 58 under 35 USC § 103(a) as being unpatentable over Carpenter, and further in view of Uchikawa (U.S. 6,531,661) and Asai (U.S. 6,534,723).

Claims 45-46

As part of making the rejection, the Examiner states at page 7 of the Final Office Action that "Carpenter discloses all the features of the claimed invention as applied to claim 40 above." Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" or "the third conductive layer including a second via that extends through the third dielectric layer" as recited in claim 40.

Claims 45-46 depend from claim 40 such that claims 45-46 incorporate all of the limitations of claim 40. Since Uchikawa et al. and Asai also do not include these limitations, claims 45-46 are allowable for the reasons provided above with regard to claim 40.

Reconsideration and allowance of claims 45 and 46 are respectfully requested.

Claims 52, 53, 57 and 58

The Examiner further states at page 9 of the Final Office Action that "Carpenter discloses all the features of the claimed invention as applied to claim 47 above . . ." Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" or "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers" as recited in claim 47.

Claims 52, 53, 57 and 58 depend from claim 47 such that claims 52, 53, 57 and 58 incorporate all of the limitations of claim 47. Since Uchikawa et al. and Asai also do not include these limitations, claims 52, 53, 57 and 58 are allowable for the reasons provided above with regard to claim 47.

8. SUMMARY

For the reasons argued above, claims 40-58 were not properly rejected under § 102(e) and § 103(a) as being unpatentable over the cited references.

It is respectfully submitted that the art cited does not render the claims anticipated or obvious and that the claims are patentable over the cited art. Reversal of the rejections and allowance of the pending claims are respectfully requested.

Respectfully submitted,

DAISUKE KAWAGOE

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(262) 646-7009

By /Andrew Peret/
Andrew R. Peret
Reg. No. 41,246

CLAIMS APPENDIX

40. A substrate comprising:

a first dielectric layer;

a second dielectric layer;

a first conductive layer between the first and second dielectric layers;

a third dielectric layer, the second dielectric layer being between the first and third dielectric layers;

a second conductive layer between the second dielectric layer and the third dielectric layer, the second conductive layer including a first skip via that extends through the first and second dielectric layers; and

a third conductive layer on the third dielectric layer, the third conductive layer including a second via that extends through the third dielectric layer, the second via and the first skip via being stacked on top of one another.

41. The substrate of claim 40 wherein the first skip via includes a longitudinal axis and the second via includes a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via.

42. The substrate of claim 41 wherein the first, second and third dielectric layers are formed on a core.

43. The substrate of claim 42 further comprising a fourth conductive layer between the first dielectric layer and the core.

44. The substrate of claim 40 wherein the first, second and third conductive layers are patterned conductive layers.

45. The substrate of claim 40 wherein the first skip via has a diameter between 49um and 85um and the second via has a diameter between 49um and 85um.

46. The substrate of claim 40 wherein the first skip via has a length between 58um and 92um and the second via has a length between 24um and 36um.

47. A substrate comprising:

a first dielectric layer;

a second dielectric layer;

a first conductive layer between the first and second dielectric layers;

a third dielectric layer, the second dielectric layer being between the first and third dielectric layers;

a second conductive layer between the second and third dielectric layers, the second conductive layer including a first skip via that extends through the first and second dielectric layers;

a fourth dielectric layer, the third dielectric layer being between the second and fourth dielectric layers;

a third conductive layer between the third and fourth dielectric layers; and

a fourth conductive layer on the fourth dielectric layer, the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another.

48. The substrate of claim 47 wherein the first skip via and the second skip via each include a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via.

49. The substrate of claim 47 wherein the first, second, third and fourth dielectric layers are formed on a core.

50. The substrate of claim 49 further comprising a fifth conductive layer between the first dielectric layer and the core.

51. The substrate of claim 47 wherein the first, second, third and fourth conductive layers are patterned conductive layers.

52. The substrate of claim 47 wherein the first skip via has a diameter between 49um and 85um and the second skip via has a diameter between 49um and 85um.

53. The substrate of claim 47 wherein the first skip via has a length between 58um and 92um and the second skip via has a length between 58um and 92um.

54. The substrate of claim 47 further comprising:

a fifth dielectric layer, the fourth conductive layer being between the fourth and fifth dielectric layers;

a sixth dielectric layer, the fifth dielectric layer being between the fourth and sixth dielectric layers;

a fifth conductive layer between the fifth and sixth dielectric layers;

a sixth conductive layer on the sixth dielectric layer, the sixth conductive layer including a third skip via that extends through the fifth and sixth dielectric layers.

55. The substrate of claim 54 wherein the first, second and third skip vias each include a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second and third skip vias.

56. The substrate of claim 54 wherein the first, second, third, fourth, fifth and sixth conductive layers are patterned conductive layers.

57. The substrate of claim 54 wherein the first, second and third skip via each have a diameter between 49um and 85um.

58. The substrate of claim 54 wherein the first, second and third skip via each have a length between 58um and 92um.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.